REMARKS

The Examiner's Office Action dated June 23, 2003 has been received and its contents carefully noted. Applicants respectfully submit that this response is timely filed and is fully responsive to the Office Action. Please note that claims 2, 3, 11 and 12 are amended, and, further, the title is amended as suggested by the Examiner. The claims are also further amended to place them in better U.S. claim format. Accordingly, claims 1-18 remain pending, and are believed to be in condition for allowance for at least the following reasons.

With regard to the Examiner's objection to the oath/declaration, under 37 C.F.R. 1.67(a), a review of the Declaration and Power of Attorney For Patent Application filed August 14, 2001 reveals that the Declaration is recreation of the USPTO form PTO/SB/106 which also states:

		I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.	
Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐

This PTO/SB/106 Declaration form was promulgated for use by the patent applicants in May 2000 and was approved for use through October 31, 2002. Therefore, since the Declaration and Power of Attorney For Patent Application was filed August 14, 2001, the Declaration fully complies with the requirements under 37 C.F.R. 1.63(c)(2) to identify any related foreign applications and properly states that "Priority Not Claimed" in a manner proscribed by the USPTO. As further evidence of the acceptability of the above format for identifying related foreign applications in the same blocks of a declaration in which priority is indicated as not being claimed, see also USPTO form PTO/SB/1 (also approved for use in May

2000) and discussed in MPEP Chapter 600 (at page 600-31). Therefore, the Examiner's objection is inappropriate and withdrawal of the objection to the declaration is respectfully requested.

With regard to the Examiner's formality rejection of the claims 1-18, under 35 U.S.C. 112 (second paragraph), the Applicants direct the Examiner to the instant specification at paragraphs [0028]-[0030] and [0040]-[0042], as well as Figure 1A and 2A, which clearly show that the storage capacitor is formed from several constituents of the pixel matrix circuit. That is, the storage capacitor is formed by the capacitor wiring line 203 (which is at the same device level as the first wiring layer 202a, 202b, 202c), a semiconductor region 210 (namely, a portion extended from the drain region 207, the channel region 209 and the low concentration regions 208b, 208d) and a part of the first insulating layer 204 employed as a dielectric.

Therefore, the phrase:

> storage capacitor is formed **from a capacitor wiring line formed on the same layer as the first wiring line, from a semiconductor region** that has the same composition as the channel formation region or the low concentration impurity region, and **from a part of the insulating layer**"

of claims 1, 2, 10 and 11 and the phrase:

> "the storage capacitor is formed **from a capacitor wiring line formed on the same layer as the first wiring line, from a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region**, and **from a laminate of the first insulating layer and the silicon oxide film**"

of claims 3 and 12, clearly set forth to one of ordinary skill in the prior art the subject matter which the Applicants regard as their invention based upon a reading of the specification, as proscribed in MPEP Chapter 2173.02. The Applicant's respectfully request withdrawal of the formality rejection as it relates to the above phrases.

Turning to the Examiner's formality rejection of claims 2, 3, 11 and 12, regarding the phrases "first wiring line through an insulating layer" and "first wiring line through a first insulating layer", the Applicants have amended claims 2,

3, 11 and 12 to clearly define the structure of the channel formation region of the TFT pixel as being formed by a:

> "..a first wiring line with a first insulating layer...a second insulating layer...interposed between the channel formation region and the first wiring layer"

In light of these amendments, the Applicants request that the formality rejection of claims 2, 3, 11 and 12, based upon the lack of clarity of the above phrases, be withdrawn.

With regard to the Examiner's rejections of:

> Claims 1-6, and 9, under 35 U.S.C. 103(a), as being obvious in view of the teachings of Hirabayashi et al ('019) and Hashimoto et al ('303),
>
> Claim 7, under 35 U.S.C. 103(a), as being obvious in view of the teachings of Hirabayashi et al ('019), Hashimoto et al ('303) and Someya et al ('295),
>
> Claim 8, under 35 U.S.C. 103(a), as being obvious in view of the teachings of Hirabayashi et al ('019), Hashimoto et al ('303) and Murade ('722),
>
> Claims 11 [sic 10]-18, under 35 U.S.C. 103(a), as being obvious in view of the teachings of Hirabayashi et al ('019), Hashimoto et al ('303), Seo ('068) and Murade ('722),

the Applicants respectfully each of these rejections.

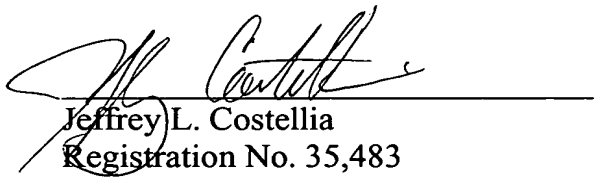
The Applicants initially assert that the basic combination of Hirabayashi et al and Hashimoto et al does not teach a storage capacitor formed from a capacitor wiring line on the same layer as the first wiring layer which is recited in all independent claims of the instant application. The Examiner asserts that Hirabayashi et al does show such feature, but a review of the patent document reveals that Hirabayashi et al, particularly Figure 3, does not teach this claimed feature. That is, the patentees teach that the capacitor 70 is formed by the capacitor line 3b (which include both elements 3b illustrated, one capacitor line 3b above the immediate capacitor electrode 1f and one capacitor line 3b connected to the previous or subsequent pixel. The gate electrode (scanning line) 3a is at the same level as the capacitor lines 3b, but there is no storage capacitor formed from a capacitor line on the same layer as a first wiring layer which formed below the channel region of the TFT presently claimed. In contrast to the claimed invention,

the wiring lines 3a and 3b of Hirabayashi et al are formed above the channel region 1a (see Figure 3; paragraphs [0092]-[0096] and [0103]-[0105]).

Further, a review of the supporting references to Hashimoto et al, Murade, Seo and Someya reveals that none of those documents remedies the deficiency of Hirabayashi et al by teaching a capacitor formed from a capacitor wiring line on the same layer as the first wiring layer, such that even if combined, the proposed combination would not satisfy the requirements of § 103(a) for setting forth a *prima facie* case of obviousness by teaching or suggesting each and every feature of the claimed invention. Consequently, the rejection of claims 1-18, under § 103(a) , based upon the combination of the Hirabayashi et al reference with the Hashimoto et al, Murade, Seo and Someya references must be withdrawn.

Having responded to all objections and the rejection set forth in the outstanding Office Action, it is submitted that claims 1-18 are in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,



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